PCT/GB 99/04245
15 DECEMBER 1999

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16DEC98 E412204-1 D02000
F01/7700 0.00 - 9827612.4

15 DEC 1993

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference — PDG/21095

2. Patent application number *(The Pate* — 9827612.4 — 15 DEC 1998

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

SNELL & WILCOX LIMITED
6 Old Lodge Place
St Margaret's
Twickenham
Middlesex TW1 1RQ

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — UNITED KINGDOM

55 19764005

4. Title of the invention

Encryption of Digital Video

5. Name of your agent *(if you have one)*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

MATHYS & SQUIRE

100 Gray's Inn Road
London WC1X 8AL
UNITED KINGDOM

Patents ADP number *(if you know it)* — 1081001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

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9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	-
Description	3
Claim(s)	1
Abstract	-
Drawing(s)	2 +2 -10

10. If you are also filing any of the following, state how many against each item.

Priority documents	-
Translations of priority documents	-
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	-
Request for preliminary examination and search *(Patents Form 9/77)*	x
Request for substantive examination *(Patents Form 10/77)*	-
Any other documents *(please specify)*	-

11. I/We request the grant of a patent on the basis of this application.

Signature MATHYS & SQUIRE Date 15 Dec 1998

12. Name and daytime telephone number of person to contact in the United Kingdom: Peter D Garratt - 0171 830 0000

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Notes

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Encryption of Digital Video

This invention concerns digital outputs from devices for playing pre-recorded digital video media such as Digital Versatile Disks (DVD). Suppliers of video programme material are concerned to avoid the creation of unauthorised "pirate" copies by connecting the output of a player to a recorder. There are known methods of modifying an analogue video signal to make it unsuitable for recording without affecting the ability of a display device to show the picture; an example is the "Macrovision" system which modifies the field synchronising signals amongst other things. However, the advent of digital technology has made it possible to create copies which are undistorted replicas of the original programme. For this reason suppliers of digital consumer equipment are often contractually required not to provide digital outputs which are capable of being recorded by unauthorised persons.

Professional video equipment almost invariably uses the digital interfaces defined by the ITU/R in their Recommendation 656. These interfaces handle uncompressed digital component (i.e. luminance and colour difference) signals and integrated circuits which support the bit-serial version are readily available. There are thus many advantages to the use of Rec. 656 interfaces in consumer equipment; however, such use could contravene contractual requirements relating to the provision of recordable digital outputs.

The inventor has appreciated that the parallel and serial digital component interfaces defined in ITU/R Recommendation 656 can be modified to prevent unauthorised use of the digital signal by sending the timing reference signals (TRSs) infrequently, typically once per frame, and by omitting some or all of the blanking and field phase information from the TRSs. Suitably the TRS can be placed other than at the start or finish of a digital active line.

In a further aspect of the invention the transmitted TRSs include additional information about the video, such as its line standard or aspect ratio, or data to confirm the validity of the signal.

Advantageously the order of the bits in the digital words is rearranged, either in a fixed pattern or in a changing pattern synchronised by the transmitted timing reference signals.

In a normal digital component signal in accordance with ITU/R Rec. 656 the TRSs are sent twice per line, and they enable a receiving device, such as a recorder, to identify the order of the words in the multiplex of luminance and colour difference words, and, in the case of the bit-serial interface, they enable the boundaries of the data words to be identified. As well as marking the start and finish of each line the TRSs identify the start and end of each field and frame.

Existing digital equipment relies for its proper operation on the presence of TRSs at the start and finish of each digital active line and will fail to operate if they are absent. However, if the line standard of the signal is known, the timing reference signals can be regenerated from the data clock if the position within the frame of one clock pulse is known. Provided a continuous clock signal is present, a single start- or end-of-field

TRS enables all the information normally carried by the regular TRSs to be regenerated.

An example of the invention will now be described with reference to the drawings in which:

Figure 1 shows the block diagram of a video encryption system.

Figure 2 shows the block diagram of a video decryption device

Referring to Figure 1, a digital video source (1) outputs a parallel (8 bits and clock) signal having the format defined in ITU/R Rec. 656. This signal feeds a digital sync separator (2) and a TRS remover (3). The separator recognises the TRSs in the input signal and decodes the following signals from them: digital line blanking (H), digital field blanking (V) and field phase (F). The TRS remover replaces the TRSs by data corresponding to blanking levels.

The video data without TRSs goes to a modified TRS inserter (4) which inserts a modified TRS once per frame at a fixed point in the video blanking. The modified TRS consists of four data words followed by a further four validation words as follows (in hexadecimal notation):

FF 00 00 IJ $V_{11}V_{12}$ $V_{21}V_{22}$

The validation words are fixed and identify the method of encryption. The IJ word has its four most significant bits as shown in the table below and the four least significant bits are error detection bits defined in the same way as in the XY word of the TRS described in Rec. 656.

Bit	Value
7	1
6	0
5	0 for 16:9 aspect ratio 1 for 4:3 aspect ratio
4	1 for 625 lines 0 for 525 lines

The output of the inserter drives a bit rearranger (5) which changes the order of the bits in the word in a changing pattern synchronised by the field phase signal. The resulting signal can be output directly as an encrypted parallel signal (6), or passed to a standard Rec. 656 Serialiser (7), which converts the parallel data into a bit-serial stream exactly as described in Rec. 656, to provide an encrypted serial signal (8).

Figure 2 shows a video decryption device. An encrypted serial digital signal (8) is fed to a standard Rec. 656 deserialiser (21) to provide a parallel data and clock signal to a bit order rearranger (22). Alternatively, if a parallel encrypted signal (6) is already available, it can be fed directly to the rearranger (22).

The output of the rearranger feeds a TRS detector and decoder (24). The TRS is detected in the conventional manner from its FF and 00 words, which are unaffected by the bit reordering.

The TRS detector outputs a synchronising pulse (23) when a valid TRS is detected. The line standard and aspect ratio are also decoded from the relevant bits of the TRS.

The synchronising pulse synchronises a sync pulse generator (25), which is set to the appropriate line standard by the decoded line standard information and driven from the word-rate clock to generate F, V and H signals which are correctly timed to the video data.

The bit-order rearranger (22) restores the correct order of the bits by the reverse of the process (5) in the encrypter. The changing pattern of bit order changes is synchronised by the synchronising pulse (23), which occurs at a fixed position relative to the start of each frame. The resulting parallel digital video signal drives a TRS inserter (26) which inserts standard Rec. 656 TRSs in response to the F, V and H signals from the SPG (25). The resulting decrypted parallel signal can be output directly for use (27), or serialised in accordance with Rec. 656 in Serialiser (28). It should be noted that the TRS insertion is only necessary if a "standard" signal is required for subsequent processing. In most applications only the output video data from the TRS detector (24) and the F, V and H signals from the sync pulse generator (25) will be required.

The above description has been based on eight-bit processing but the skilled man will appreciate that Rec. 656 explains how ten-bit signals are carried by the serial and parallel interfaces and that these methods are directly applicable to the subject matter of the invention.

It must be recognised that the invention has been described only by way of example and many variations are possible within the concepts described. For example the contents and frequency of transmission of the TRSs could differ from that described here.

Claims

1. A digital video interface substantially in accordance with ITU/R Recommendation 656 characterised in that timing reference signals are transmitted less than twice per line in order to prevent unauthorised use of the video information.
2. A digital video interface as described in Claim 1 where any timing reference signal does not correspond to the start or finish of a digital active line.
3. A digital video interface in accordance with either Claim 1 or Claim 2 in which the fourth word of any TRS does not contain F, V and H information in accordance with Rec. 656.
4. A digital video interface in accordance with either Claim 1 or Claim 2 in which aspect ratio information is carried in the timing reference signals.
5. A digital video interface in accordance with either Claim 1 or Claim 2 in which line standard information is carried in the timing reference signals.
6. A digital video interface in accordance with either Claim 1 or Claim 2 in which the timing reference signals include data identifying a method of encryption.
7. A digital video interface in accordance with any of the preceding claims in which the order of significance of the bits is rearranged.
8. A digital video interface in accordance with any of the preceding claims in which the order of significance of the bits is rearranged according to a predictable pattern.
9. Video encryption apparatus in accordance with any of the preceding claims 1 - 8.
10. Video decryption apparatus in accordance with any of the preceding claims 1 - 8.

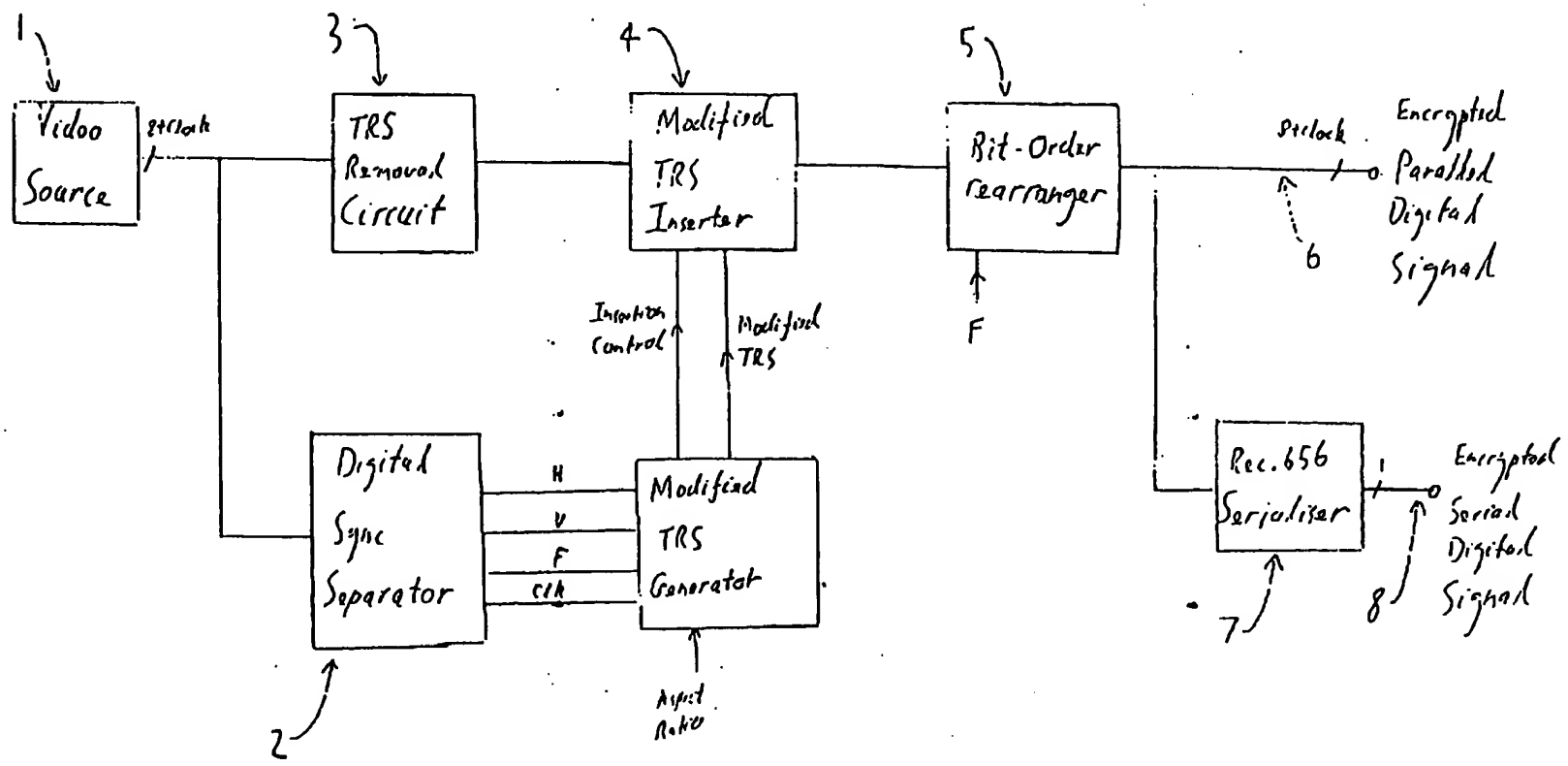

Figure 1 Video Encryption System

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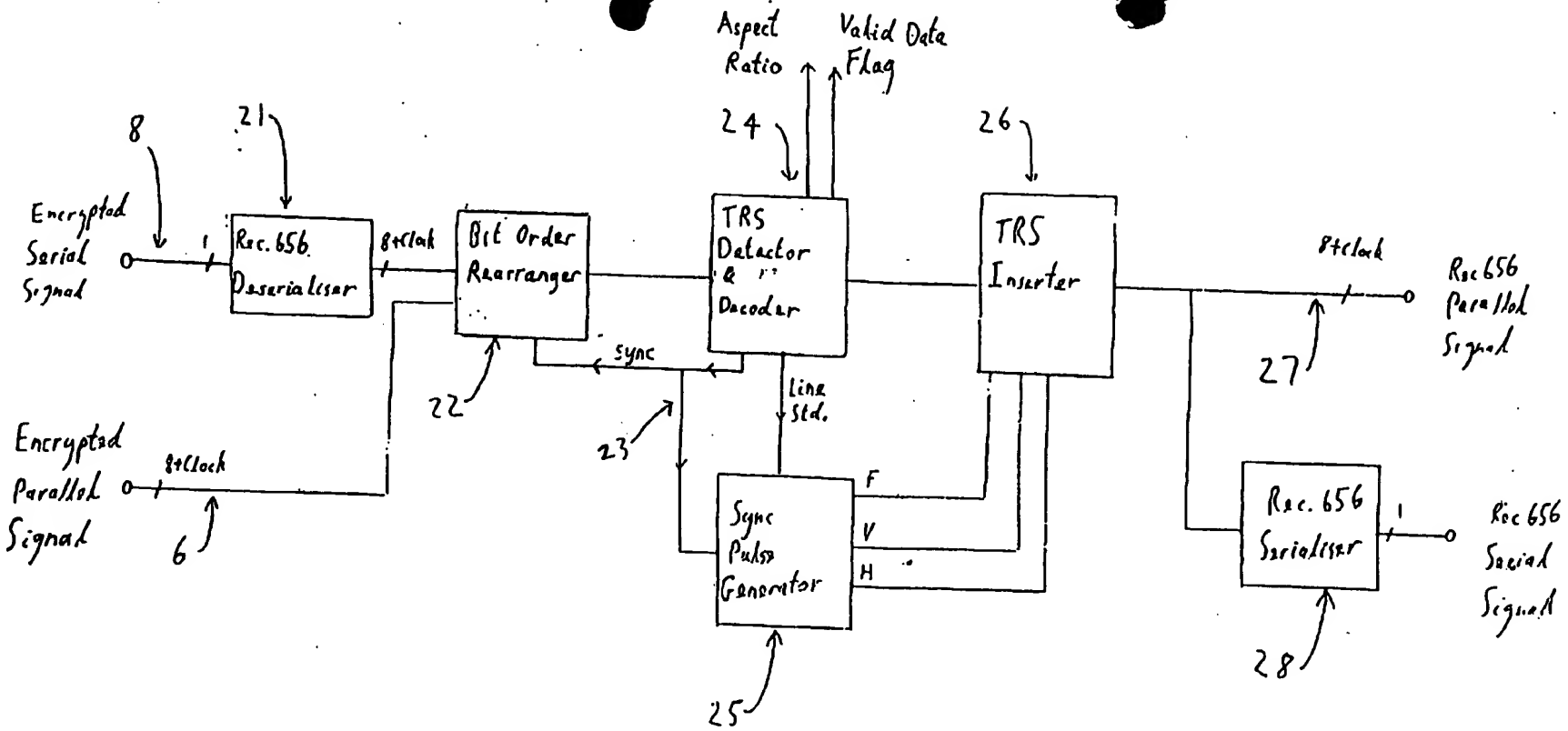

Figure 2 Video Decryption System

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